INVESTOR BRIEFING

Neural Decoder System for Fault-Tolerant Quantum Computing

Technical Differentiation, Industrial Integration & Investment Relevance

European Business Group
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A closed loop—not another point decoder.

Integrated neural decoding can compress commissioning cycles while improving adaptation, control latency and operational safety.

INVESTMENT PROPOSITION

Innovative Solution

Universal backbone + chip adapter + drift compensation + deterministic deployment + fallback gating.

Further steps

Performance, commissioning-time and commercial-impact metrics will be demonstrated on target hardware.

Error correction must decide before the next cycle.

Today’s decoders trade one constraint for another.

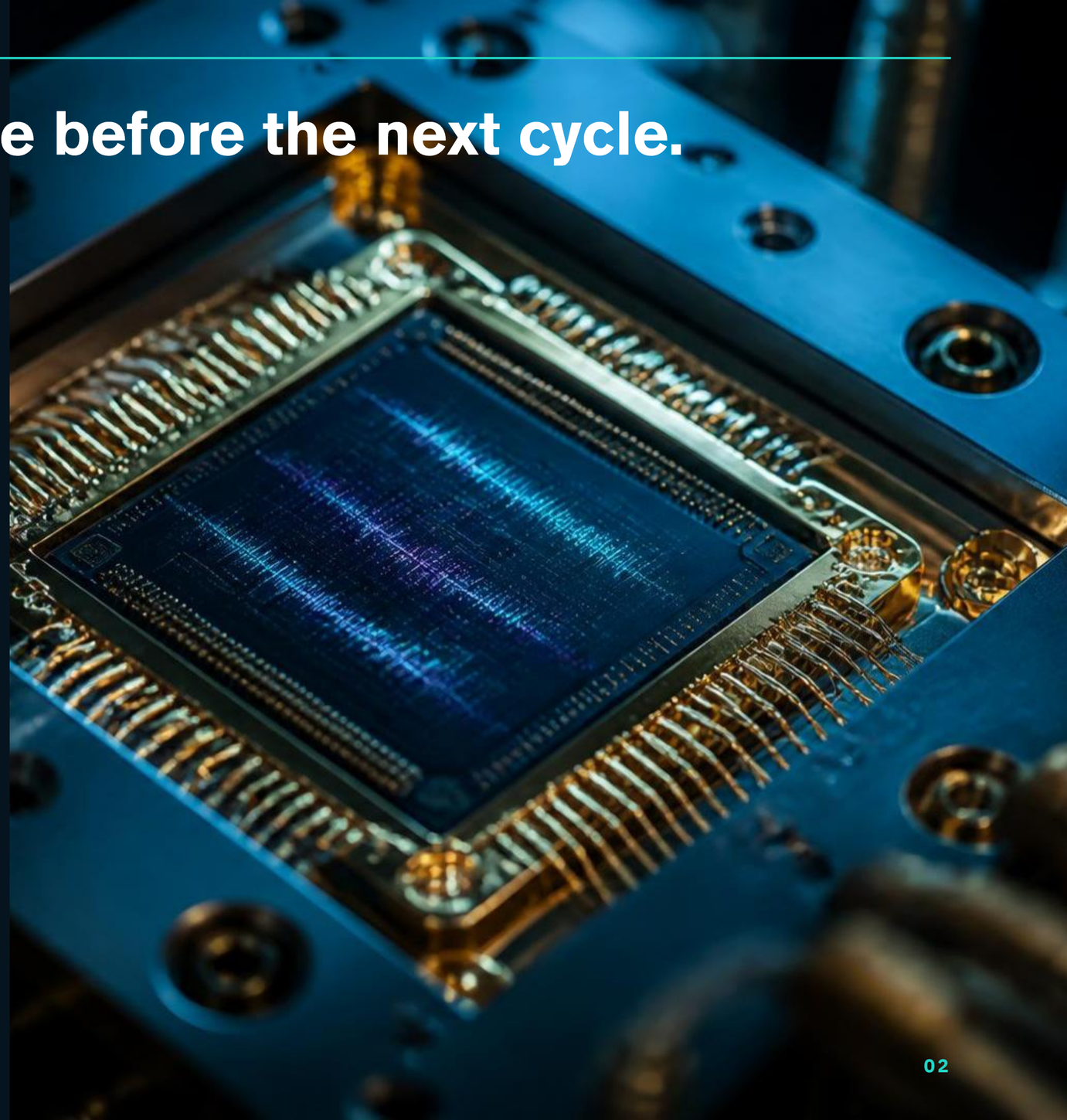
Accuracy ↔ latency

Generality ↔ device specificity

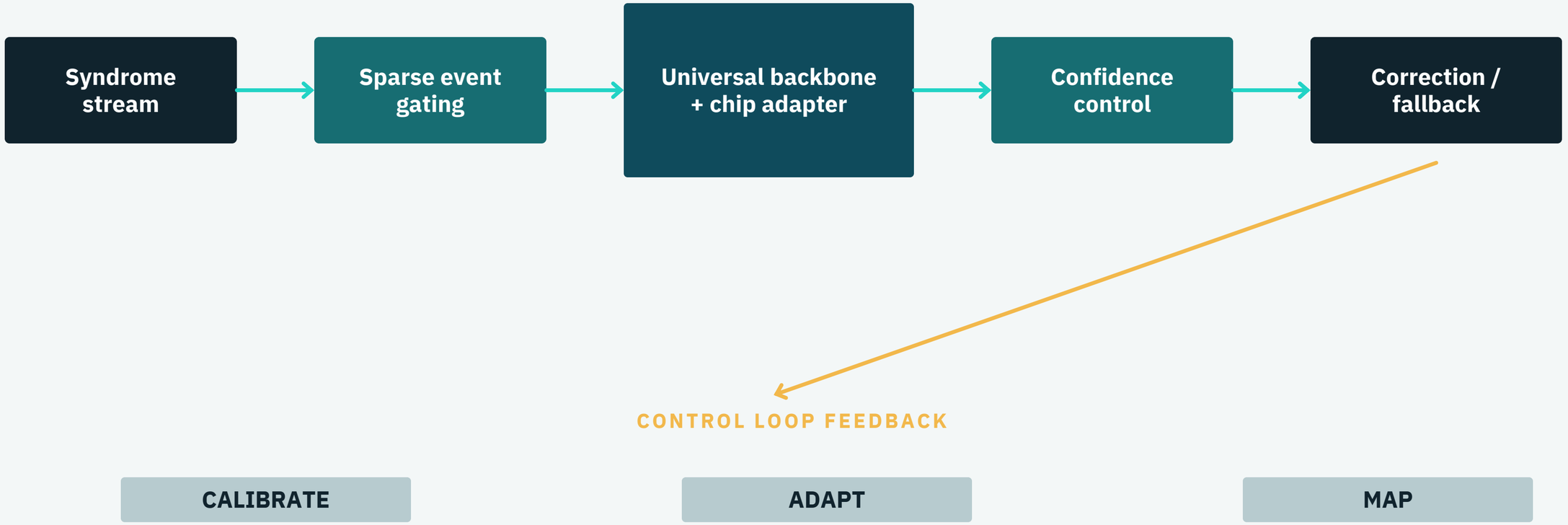
Adaptation ↔ retraining overhead

Autonomy ↔ safe fallback

Fragmentation raises commissioning cost and compound reliability risk as systems scale.



Integrated neural decoder architecture



Universal knowledge. Minimal device-specific change.

UNIVERSAL BACKBONE

Learns syndrome–error structure across processors, code families and noise models.

CHIP ADAPTER

Modulates a bounded parameter set for crosstalk, drift and readout effects—without full retraining.

Protected updates: shadow evaluation → confidence gate → promote or rollback

Spend compute only where the syndrome demands it.

01 SELECT

Gate by uncertainty, age and calibration drift

→

02 ATTEND

Sparse attention preserves long-range correlations

→

03 AGGREGATE

Local graph messages resolve neighborhood structure

→

04 EXECUTE

Quantised event path meets cycle budgets

Design intent: bounded memory traffic ▪ parallelizable neighborhoods ▪ deterministic scheduling

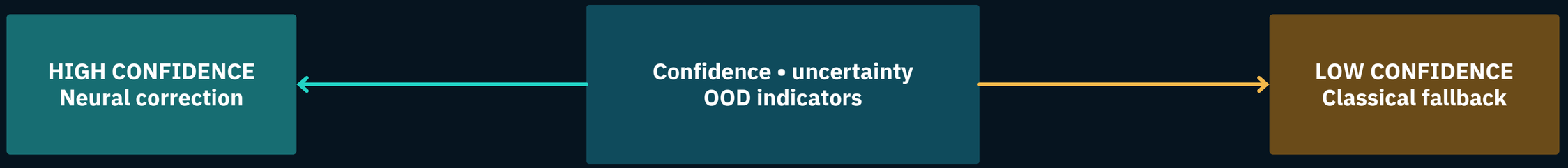
Compiler mapping turns model sparsity into hardware determinism.

OPTIMIZATION TARGETS

Latency Memory Area Power

Distributed local decoder nodes extend the same compilation contract across modular systems.

Confidence is a control signal—not a dashboard metric.



Update gating

Only trusted observations enter drift compensation.

Hybrid teacher–student

Classical supervision supports auditability and deployment robustness.

Rollback

Protected promotion prevents unsafe adapter updates.

One decoder architecture, six deployment vectors.

01
Surface-code decoding

02
New-chip commissioning

03
Online drift compensation

04
Distributed modular decoding

05
Accelerator compiler targets

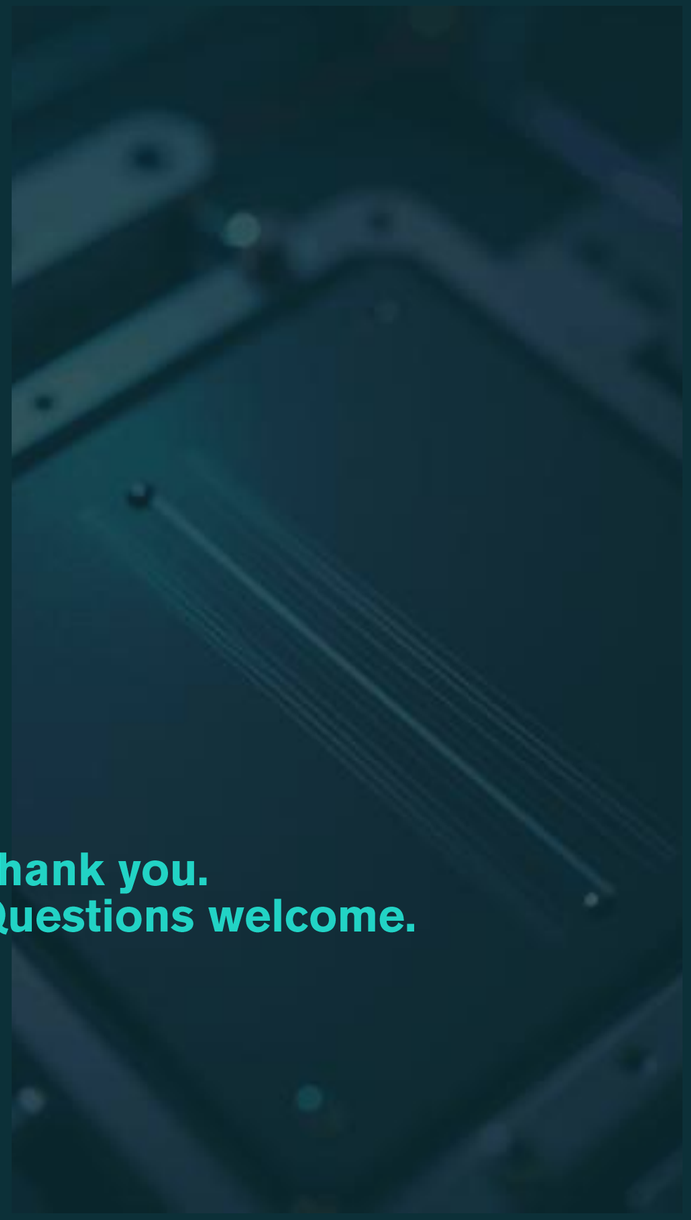
06
Explainable hybrid models

INVESTMENT DISCUSSION

From decoder prototype to control-stack standard.

An integrated architecture aimed at the central bottleneck in scalable quantum computing.

NEXT **Pilot collaboration • diligence data room**



Thank you.
Questions welcome.

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