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automation in silicon

**Single-chip PLC for STEP7** from Siemens

# PLC7100

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## Single-chip PLC for STEP7 from Siemens

The PLC7100 is the latest member of profichip's successful SPEED7 PLC processor family. Though based on its well-known predecessors the PLC7100 goes one step ahead: apart from an external DRAM and a non-volatile boot media it combines all the necessary system components to build a STEP7 programmable PLC CPU on a single piece of silicon. Equipped with a rich set of direct IO and communication features the PLC7100 is suited perfectly well to replace proprietary solutions by a new generation of single-chip PLCs supporting a popular and widely-used PLC programming language, tool chain and service capabilities.

### Direct I/O Functions

The PLC7100 provides a maximum number of 24 digital inputs and 16 digital outputs. Besides the standard I/O functionality versatile interface features are available: the inputs can be configured to trigger an alarm with very low latency or to carry out various hardware counter functions like up/down, A/B for rotary encoders or frequency and pulse measurement. Functions like 4 channel Pulse-Width-Modulation or Stepper Motor Control and an SSI interface round up the very flexible I/O capabilities. Due to sharing common interface pins some restrictions apply which I/O functions can be used simultaneously but no matter which I/O functions are selected all inputs and outputs are mapped directly into the PLC process image resulting in very low latency and fast access times.
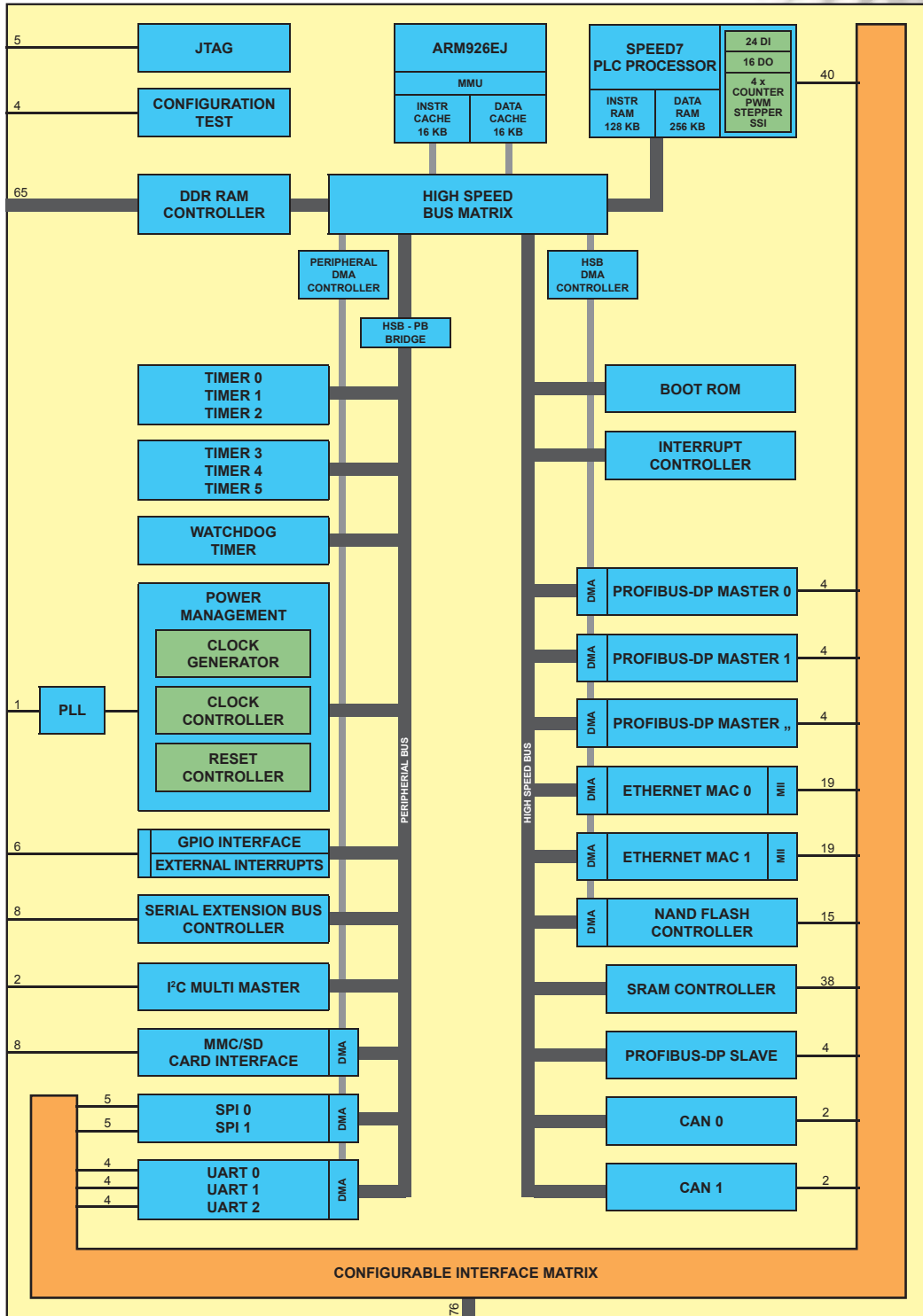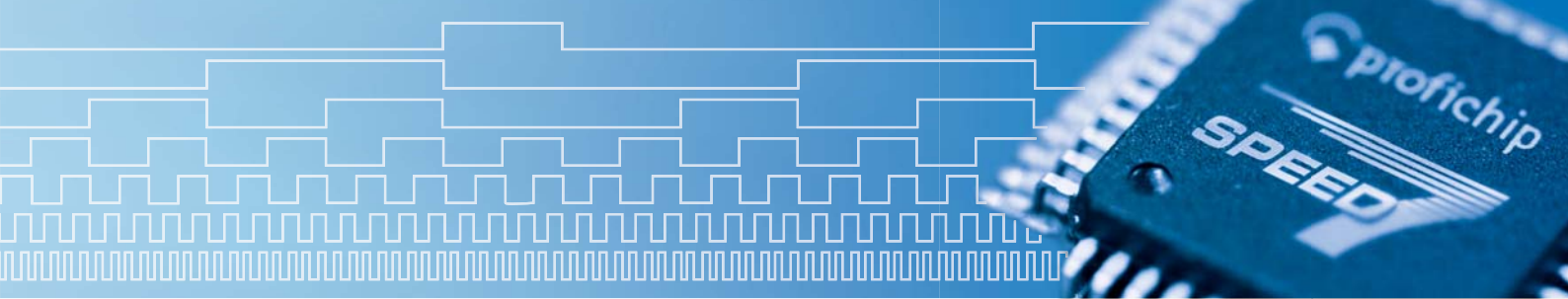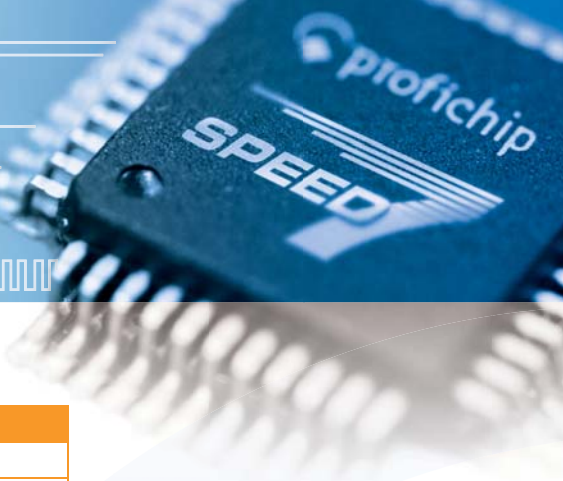
### Communication Interfaces

The PLC7100 leaves almost nothing to be desired with respect to industrial communication. Three Profibus-DP masters are tailor-made for the PLC7100 system architecture and can be additionally used for MPI communication, profichip's well-known VPC3+C Profibus slave supporting all DPV0, DPV1 and DPV2 services and two CAN interfaces with flexible message box and FIFO modes ensure a seamless connectivity to the most important fieldbus protocols worldwide. The two 10/100 Ethernet-MACs can be used for PG/OP communication, standard Ethernet protocols or Ethernet-based industrial communication protocols. Numerous serial standard interfaces like three UARTs, two SPI channels, an I2C Multi-Master-Interface along with an SD/MMC and a NAND-Flash interface to connect non-volatile boot and backup memories complete the broad range of communication features. The communication concept is very flexible and there are few restrictions on using several interfaces simultaneously due to shared pins.

### Software Support

The S7 operating system and the communication stacks are running on the integrated ARM926EJ Processor with 16kB/16kB cache. Together with cooperation partners profichip will offer different software packages for the chip. Depending on their requirements customers can choose from a set of pre-configured software bundles which are then licensed with the chip. User applications are recommended to be written in STEP7; directly programming the ARM processor is not supported.

For writing and debugging the STEP7 program all the available standard tools can be used. Debug features like single-stepping, setting breakpoints and real-time watching are supported by the PLC7100. Download of the MC7 code as well as using online functions is possible via MPI interface or by using an Ethernet Port in PG/OP mode. Alternatively the PLC program can be stored on a non-volatile media (SD/MMC or NAND-Flash) for initial download or backup.

JTAG

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CONFIGURATION TEST

4

DDR RAM CONTROLLER

65

ARM926EJ

MMU

INSTR CACHE 16 KB | DATA CACHE 16 KB

SPEED7 PLC PROCESSOR

INSTR RAM 128 KB | DATA RAM 256 KB

24 DI
16 DO
4 x COUNTER PWM STEPPER SSI

40

HIGH SPEED BUS MATRIX

PERIPHERAL DMA CONTROLLER

HSB DMA CONTROLLER

HSB - PB BRIDGE

TIMER 0
TIMER 1
TIMER 2

TIMER 3
TIMER 4
TIMER 5

WATCHDOG TIMER

POWER MANAGEMENT

CLOCK GENERATOR

CLOCK CONTROLLER

RESET CONTROLLER

PLL

1

GPIO INTERFACE
EXTERNAL INTERRUPTS

6

SERIAL EXTENSION BUS CONTROLLER

8

I²C MULTI MASTER

2

MMC/SD CARD INTERFACE

8

DMA

SPI 0
SPI 1

5
5

DMA

UART 0
UART 1
UART 2

4
4
4

DMA

PERIPHERIAL BUS

HIGH SPEED BUS

BOOT ROM

INTERRUPT CONTROLLER

DMA | PROFIBUS-DP MASTER 0 | 4

DMA | PROFIBUS-DP MASTER 1 | 4

DMA | PROFIBUS-DP MASTER „ | 4

DMA | ETHERNET MAC 0 | MII | 19

DMA | ETHERNET MAC 1 | MII | 19

DMA | NAND FLASH CONTROLLER | 15

SRAM CONTROLLER | 38

PROFIBUS-DP SLAVE | 4

CAN 0 | 2

CAN 1 | 2

CONFIGURABLE INTERFACE MATRIX

76

# Features:

| Features | PLC7100 | PLC7200 |
|---|---|---|
| PLC Assembler Code | MC7 | MC7 |
| PLC Memory (Data/Instruction) | 256kB / 128kB | 16MByte [3] |
| System Interfaces [1] | | |
| SRAM Interface | 8/16Bit x 64k | 8/16Bit x 64k |
| On-Chip I/Os | 24DI / 16DO | 24DI / 16DO [3] |
| Alarms (e.g. OB 40) | 16 | 16 [3] |
| Counter (Up, Down, A/B, etc.) | 4 x 32Bit | 4 x 32Bit [3] |
| PWM , Stepper Control | 4 | 4 [3] |
| SSI In/Out-Master | 1/1 | 1/1 [3] |
| General Purpose I/Os | 6 | 6 |
| ser. Extension Bus P-Bus/HSB | ✓/✓ | ✓/✓ |
| Communication Interfaces [1] | | |
| PROFIBUS-DP master / MPI (12MBit/s) | 1 | 3 |
| PROFIBUS-DP slave (12MBit/s) | 1 | 1 |
| CAN 2.0 A/B | 2 | 2 |
| Ethernet 10/100 | 1 | 2 |
| Standard Serial (UART) | 2 | 3 |
| Serial Peripheral Interface (SPI) | 2 | 2 |
| $I^2C$ Multi-Master | 1 | 1 |
| SD / MMC Interface | 1 | 1 |
| NAND-Flash Controller | 1 | 1 |
| PLC System Counter and Timer | | |
| Instruction Cycle Time | 20nsec | 5nsec |
| Counter | 2048 | 2048 |
| Timer 10 msec. min | 2048 | 2048 |
| High-Resolution Timer 1µsec. | n [2] | n [2] |
| IEC Timer | max [2] | max [2] |
| RTC (no backup) | ✓ | ✓ |
| Technical Data | | |
| Core Supply Voltage | 1,2V | 1,2V |
| I/O Voltage | 3,3V / 2,5V | 3,3V / 2,5V |
| Clock Supply (Crystal Oscillator) | 48MHz | 48MHz |
| Max. Power Consumption | < 1,3W | ~ 1,5W |
| Temperature Range | -40°C - +85°C | -40°C - +85°C |
| Package | BGA 256, Pitch 1,0 mm | BGA, Pitch 1,0 mm |

1) The listed values represent the total number of integrated interfaces. Depending on the system configuration not all interfaces can be used simultaneously.
2) Limited by available memory only.
3) Depending on external interface