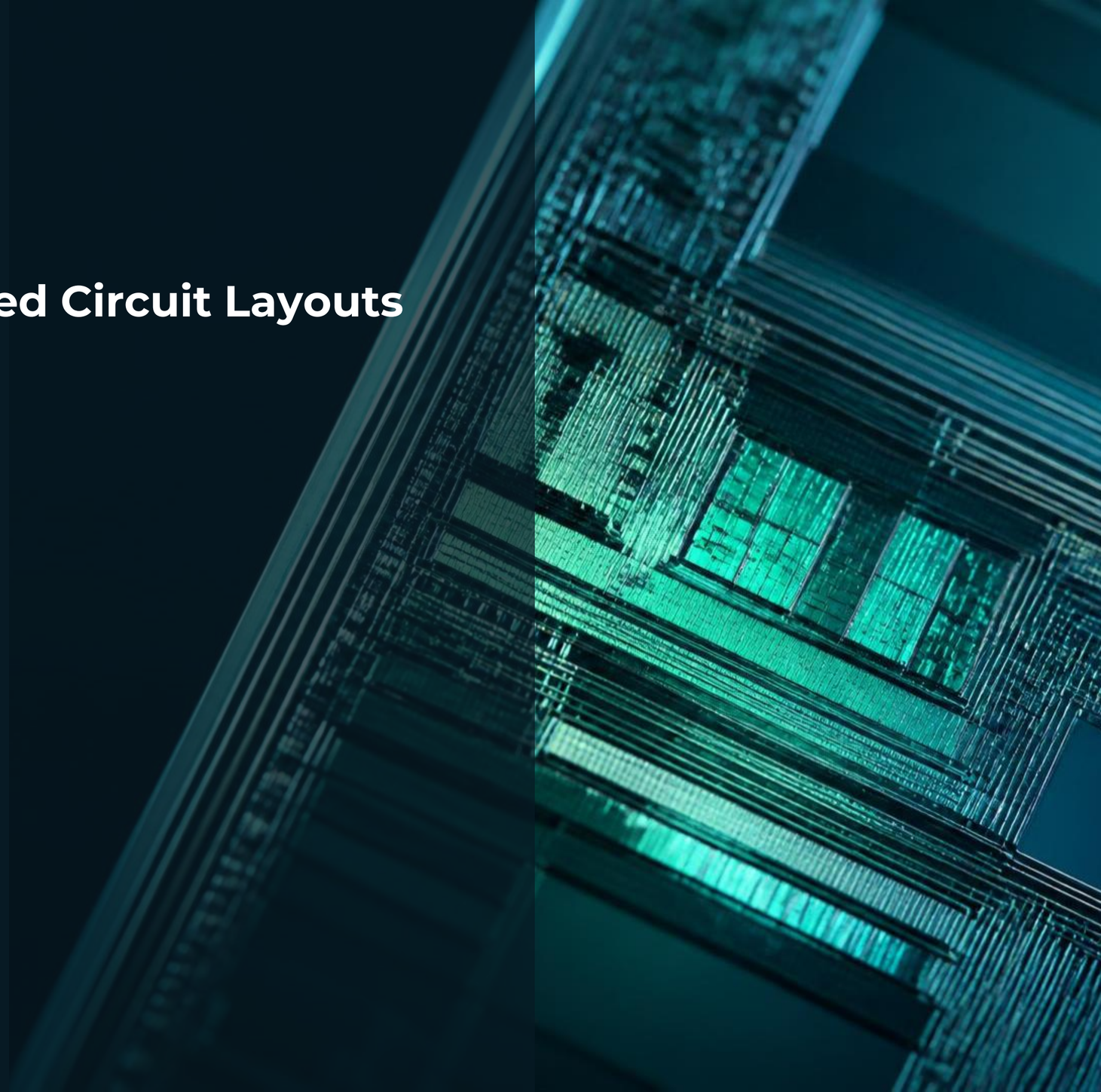
INVESTOR PRESENTATION · DEEP TECH

Closed-Loop AI-EDA for Integrated Circuit Layouts

Technical Differentiation and Industrial Integration



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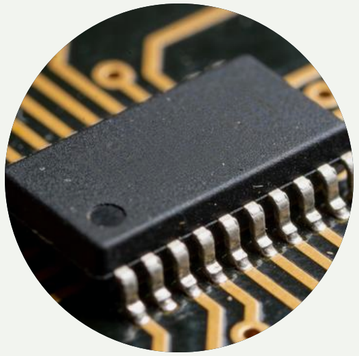
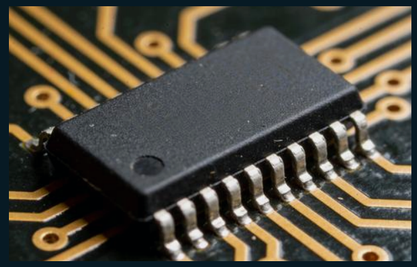
From a sequential flow to a traceable loop.

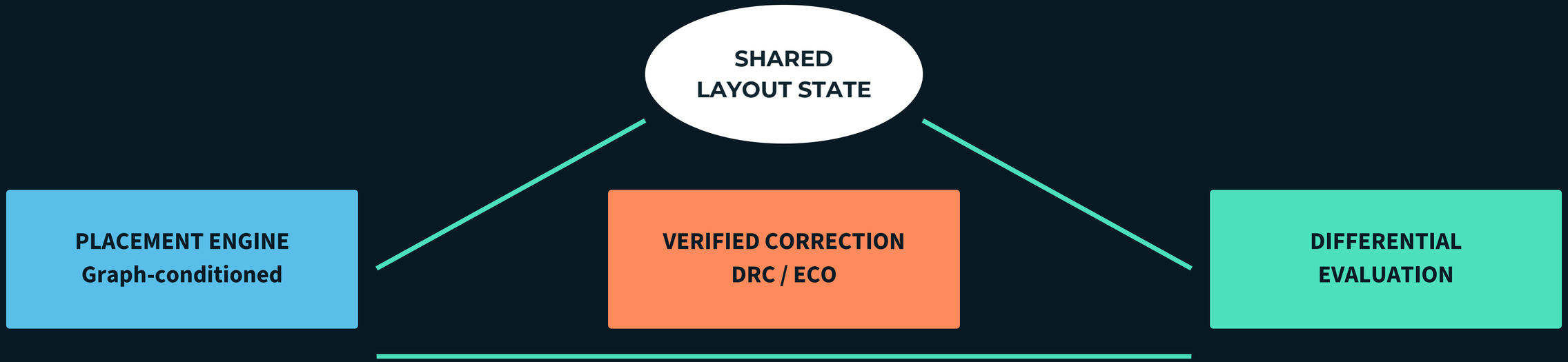
Problem: Placement, correction and evaluation are separated. Solution: a shared layout state with verified, incremental feedback.

- Repeated full-chip analyses
- Lack of traceability
- Late risk detection
- Unsafe automated repairs



One state. Three engines. One auditable loop.





Versioned data model:

Layout-State ID · Differential Layout Record · Correction Record · Transaction ID · Rollback Pointer · Confidence · Provenance

03 · DIFFERENTIATION

Technical coupling instead of isolated AI.

SEQUENTIAL EDA FLOW

Placement → Correction → Evaluation

Full-chip re-evaluation

Manual / isolated ECOs

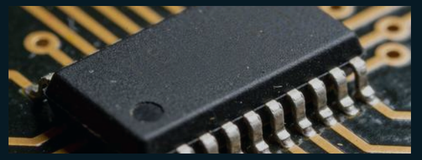
CLOSED-LOOP ARCHITECTURE

Shared state + feedback

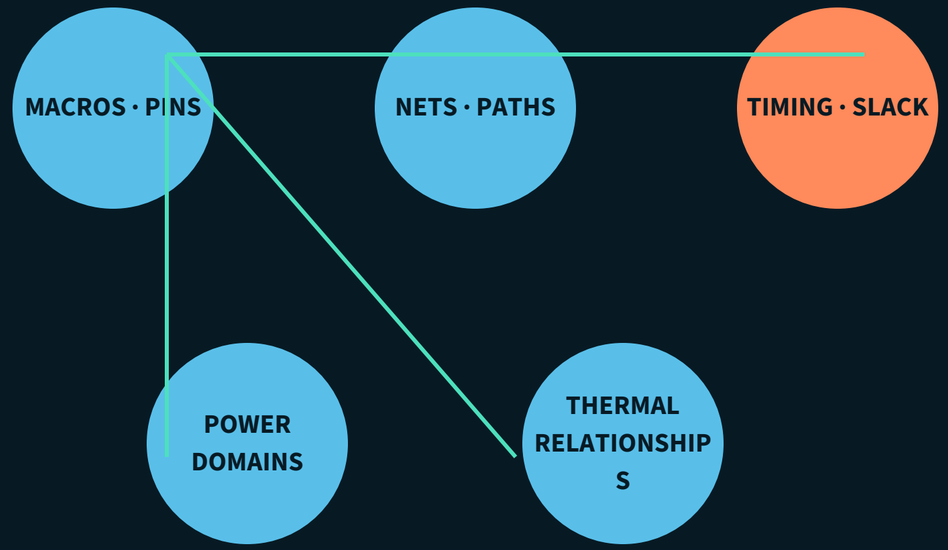
Incremental evaluation

Verified + traceable

Graph data drives the diffusion process.



Graph: Macros, pins, nets, timing paths, power domains, thermal relationships and floorplan constraints. Cost: wirelength, overlap, congestion, timing slack, power density, thermal risk and design-rule risk.

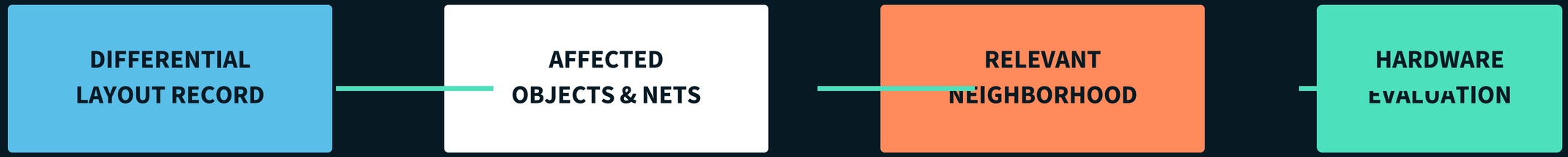


COST: Wirelength · Overlap · Congestion · Slack · Power · Thermal · DRC Risk
Validation required: Quality · Scalability · Convergence · Baselines

Automate — with a safety proof.

Only formally checked candidates are executed; at low confidence: rollback, manual review or full sign-off analysis.

Compute where something actually changes.



OUTPUT

Layout Quality Value · Confidence Value · Critical Object IDs
Calibration and acceptance logic to be defined

Introduce modularly. Keep sign-off intact.

Path: 1) differential evaluation 2) verified DRC / ECO correction 3) placement coupling. Interfaces: EDA host, DRC, timing, power, routing and sign-off.

1 DIFFERENTIAL EVALUATION
Lower-risk entry point

2 VERIFIED DRC / ECO CORRECTION
Safety and traceability

3 PLACEMENT COUPLING
Closed-loop control

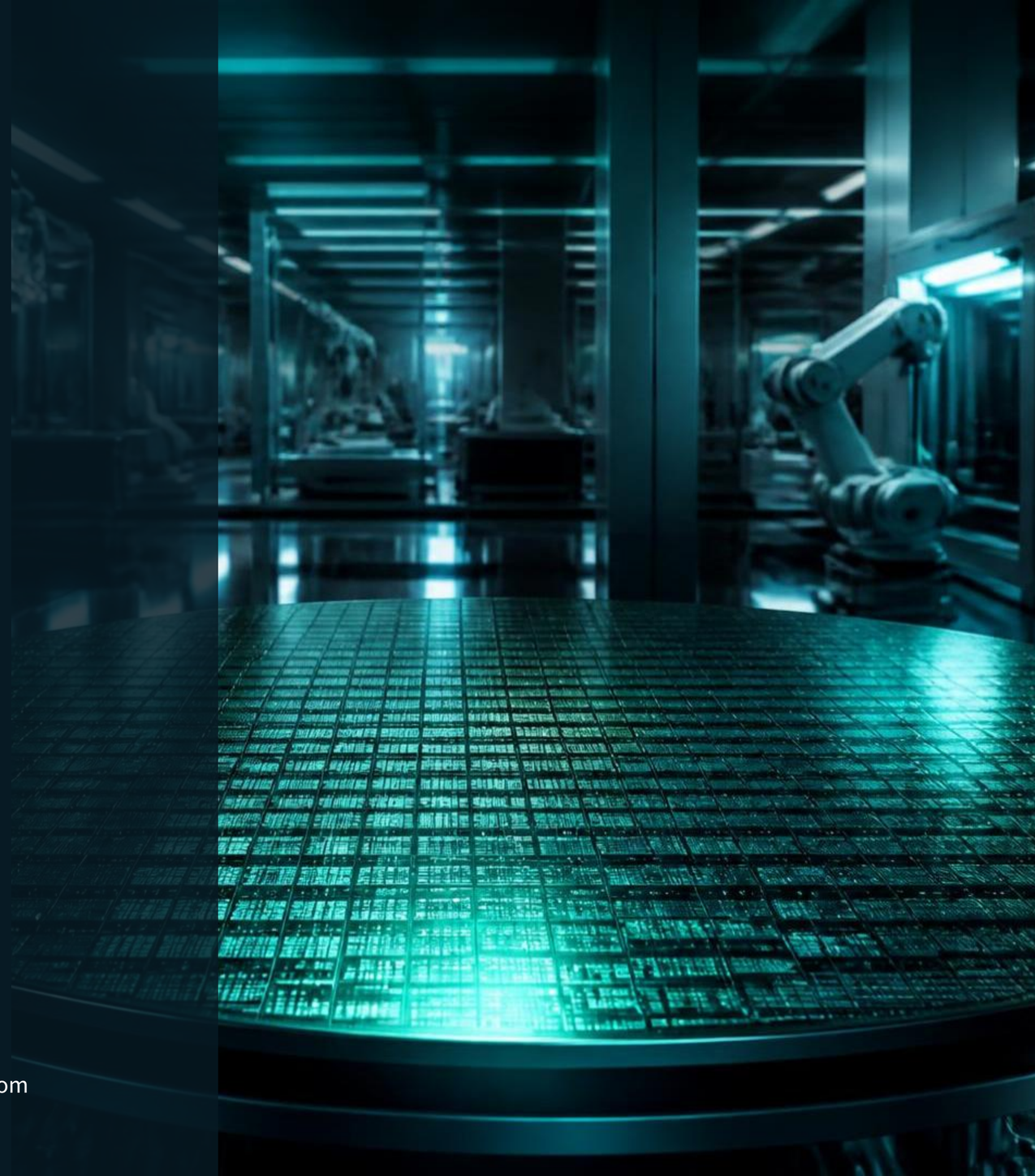
On-premises · Private cloud · Hybrid
Approval gates and conventional sign-off tools remain in place.

Beachhead first. Expansion thereafter.

BEACHHEAD
Semiconductor design houses · EDA partners
iterative SoC / ASIC flows

EXPANSION
Foundries · AI / HPC · Automotive · Chiplets ·
Advanced packaging · 3D IC

Use cases → buyer value: differential evaluation → shorter analysis paths; verified correction → controllable ECOs; placement coupling → traceable iterations. Market sizes and customers remain open.



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